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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/822,713	03/30/2001	Andrew J. Thurston	M-8319 US	7267
33031	7590	10/21/2004	EXAMINER	
CAMPBELL STEPHENSON ASCOLESE, LLP 4807 SPICEWOOD SPRINGS RD. BLDG. 4, SUITE 201 AUSTIN, TX 78759			CRAIG, DWIN M	
			ART UNIT	PAPER NUMBER
			2123	

DATE MAILED: 10/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/822,713

Applicant(s)

THURSTON, ANDREW J.

Examiner

Dwin M Craig

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 March 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-45 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-45 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 2, 4 & 5.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. **Claims 1-45** have been presented for Examination. Claims 1-45 have been Examined and rejected.

Specification

2. The Examiner objects to the attempt to incorporate subject matter into this application by reference to the following co-pending Applications:

1. United States patent application entitled, "Error Insertion Circuit for SONET Forward Error Correction", attorney docket no.: M-8353 US, naming Andrew J. Thurston and Douglas Duschatko as inventors and filed substantially contemporaneously with the present application;

2. United States patent application entitled, "BCH Forward Error Correction Decoder", attorney docket no.: 51-8342 US, naming Andrew J. Thurston as inventor and filed substantially contemporaneously with the present application; and

3. United States patent application entitled, "Galois Field Multiply Accumulator", attorney docket no.: M-8341 US, naming Andrew J. Thurston as inventor and filed substantially contemporaneously with the present application.

These attempts to incorporate co-pending Applications are improper because the U.S. Patent Application number is missing. The Examiner respectfully requests that the Applicant amend the specification, in response to this Office Action, to include the U.S. Patent Applications numbers for the cited cases.

Claim Interpretation

3. The claims have been given the broadest interpretation by the examiner. For the purposes of examination the examiner has determined that the “*ASCII string*” as claimed refers to a method of encoding coefficients for a polynomial that is being programmed using a hardware description language and that any “*string*” of values used for such a purpose is functionally equivalent to an “*ASCII string*.”

The Examiner notes that in a system that uses recursion, *feedback* is inherently part of the system.

The Examiner notes that in independent **Claim 26** the Applicant is claiming a *Field Error Correction (FEC) decoder*, the Examiner notes that the Applicant only provides enabling support for *Forward Error Correction decoders* in the specification and therefore will interpret the *FEC* in all of the claims to mean *Forward Error Correction* and not *Field Error Correction*.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4.1 Independent **Claims 26 and 36** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

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Specifically, the Applicant is claiming the term *Field Error Correction Decoder*, whereas the Applicant's specification only provides enabling support for the term (*Forward Error Correction Decoder*), clarification and/or amendment is required. An artisan of ordinary skill would be unable to make and/or use the claimed invention, specifically a *Field Error Correction Decoder*, without undue experimentation.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4.2 **Claims 34 and 44** recite the limitation "Forward Error Correction" in line 2 and line 2 respectively. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Independent **Claim 7** is rejected under 35 U.S.C. 102(b) as being anticipated by **Foxcraft U.S. Patent 5,818,855**.

5.1 As regards independent **Claim 7** the *Foxcraft* reference teaches, a method for implementing a circuit representing a complex polynomial equation in an ASIC (**Figure 5, Col. 1 Lines 53-55, Col. 2 Lines 18-37, Col. 8 Lines 5-13**), producing one or more parallel equations in a hardware description language (**EXAMPLE Col. 8 Lines 27+, Col. 9 Col. 10**), merging the

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parallel equations into a hardware description language (**EXAMPLE Col. 8 Lines 27+, Col. 9 Col. 10**), and implementing a Galois Field Circuit (**Figure 5, Col. 1 Lines 53-55**).

6. Independent **Claims 26 and 36** are rejected under 35 U.S.C. 102(b) as being anticipated by **Tomizawa et al. U.S. Patent 5,574,717**.

6.1 As regards independent **Claims 26 and 36** the *Tomizawa et al.* reference discloses an apparatus for performing forward error correction on serial data stream using the *SONET* protocol (**Figures 1A, 1B, Col. 2 Lines 43-67, Col. 3 Lines 1-13**), and using *Galios Field Decoding* (**Col. 4 Lines 40-55**), and using a de-multiplexor (**Figure 10, Col. 9 Lines 15-56**).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Independent **Claims 1, 16 and 19** and dependent **Claims 2-6, 8-15, 17, 18 and 20-25** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Foxcroft U.S. Patent 5,818,855** and in further view of **Oskouy et al U.S. Patent 5,673,279** and in further view of **Kao U.S. Patent 5,642,367**.

7.1 As regards independent **Claims 1, 16 and 19** the *Foxcroft* reference discloses a method of implementing a circuit representing a complex polynomial in a hardware description language (**Col. 2 Lines 18-37, EXAMPLE, Col. 7, 8, 9 & 10**), storing a plurality of “*strings*” of data in a plurality of storage elements (**Figure 5, Figure 7 Items 70, 60, 62, 64, 66, Col. 4 Lines 32-45**), where the plurality of “*strings*” represent a plurality of initial values of a circuit (**Col. 3 Lines 18-45**), storing the “*strings*” in data structures (**Col. 7, 8, 9 & 10**), where the “*strings*” represent mathematical operations (**Figure 1, Col. 4 Lines 7-67, Col. 5 and Col. 6 Lines 1-39**).

However, the *Foxcroft* reference does not expressly disclose the *simulation* of a serial communications device or *executing* the serial circuit for a *plurality of cycles*.

The *Oskiuy et al.* reference discloses simulation of a serial device, using a hardware description language and simulating forward error correction (*CRC*) calculation (**Figure 4 and Col. 2 Lines 40-57, Col. 4 Lines 53-67, Col. 5 Lines 1-27**).

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have simulated the circuit design created using a hardware description language, as disclosed in the *Foxcroft* reference because the simulation will allow the designed to “*Debug*” the design before the design is fabricated using an expensive fabrication process to create an integrated circuit.

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The *Kao* reference discloses that in order to properly simulate a *forward error correcting* circuit design that the circuit performing the calculations of a *Galois* field must operate for a plurality of cycles (**Col. 8 Lines 58-67 and Col. 9 Lines 1-18**).

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made to have a serial communications circuit perform for a plurality of cycles because, in order to calculate a *Galois* field because multiplication is performed in digital logic using shift registers and in order to shift the values inside these shift registers and *multiply* them then the shift register must be clocked a *plurality of cycles*.

7.2 As regards independent **Claim 7** please see paragraph 5.1 above.

7.3 As regards dependent **Claims 2 and 17** the *Foxcroft* reference discloses both “XOR” for addition and “AND” for multiplication (**Figure 11 and Figure 10, Col 6 Lines 35-39, Col. 7 Lines 15-17**).

7.4 As regards dependent **Claims 3, 18 and 23** the *Foxcroft* reference discloses BCH codes used in forward error correction and represented in a complex polynomial equation (**Col. 1 Lines 60-65, Col. 2 Lines 18-36**).

7.5 As regards dependent **Claim 8** the *Foxcroft* reference discloses parallel equations implemented in hardware (**Figure 5, Figure 7 items 70,60, 62, 64 & 66, Col. 3 Lines 65-67, Col. 4 Lines 1-6**).

However, the *Foxcroft* reference does not expressly disclose the simulation of a serial communications device.

The *Oskiuy et al.* reference discloses simulation of a serial device, using a hardware description language and simulating forward error correction (*CRC*) calculation (**Figure 4 and Col. 2 Lines 40-57, Col. 4 Lines 53-67, Col. 5 Lines 1-27**).

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have simulated the circuit design created using a hardware description language, as disclosed in the *Foxcroft* reference because the simulation will allow the designed to “*Debug*” the design before the design is fabricated using an expensive fabrication process to create an integrated circuit.

7.6 As regards dependent **Claims 9 and 20** the *Foxcroft* reference discloses storing a plurality of “*strings*” of data in a plurality of storage elements (**Figure 5, Figure 7 Items 70, 60, 62, 64, 66, Col. 4 Lines 32-45**), where the plurality of “*strings*” represent a plurality of initial values of a circuit (**Col. 3 Lines 18-45**).

7.7 As regards dependent **Claims 10 and 21** the *Foxcroft* reference discloses both “XOR” for addition and “AND” for multiplication (**Figure 11 and Figure 10, Col 6 Lines 35-39, Col. 7 Lines 15-17**).

7.8 As regards dependent **Claims 11 and 22** the *Foxcroft* reference does not expressly disclose simulating a circuit for a plurality of cycles.

The *Kao* reference discloses that in order to properly simulate a *forward error correcting* circuit design that the circuit performing the calculations of a *Galois* field must operate for a plurality of cycles (**Col. 8 Lines 58-67 and Col. 9 Lines 1-18**).

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made to have a serial communications circuit perform for a plurality of cycles because, in

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order to calculate a *Galois* field because multiplication is performed in digital logic using shift registers and in order to shift the values inside these shift registers and *multiply* them then the shift register must be clocked a *plurality of cycles*.

7.9 As regards dependent **Claims 5, 6 & 12** the *Foxcroft* reference discloses manufacturing an ASIC from a hardware description language implementation (**Col. 9 Lines 34-67 and Col. 10 Lines 34-55**).

7.10 As regards dependent **Claims 13 and 25** the *Foxcroft* reference does not expressly disclose circuit verification.

The *Oskouy et al.* reference discloses verifying a circuit design (**Figure 7, Col. 1 Lines 13-22, Col. 3 Lines 19-21**).

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made to verify the functioning of an ASIC during the design and simulation phase of product development because of the need to verify that the circuit design is working correctly before incurring the large cost involved in manufacturing an ASIC at a chip fabrication facility.

7.11 As regards dependent **Claim 14** the *Foxcroft* reference discloses a complex polynomial equation performing a BCH code (**Figure 5, Col. 2 Lines 18-37**).

7.12 As regards dependent **Claims 4, 15 and 24** the *Foxcroft* reference discloses merging one or more parallel equations into a hardware description language implementation of a Galois Field circuit (**EXAMPLE, Col. 7, 8, 9 & 10**), the Examiner notes that it is inherent that when using hardware description language that the editor used with the synthesis tool will allow the user to write the hardware description language listing to a file.

However, the *Foxcroft* reference does not expressly disclose removing initial register values and adding a feedback value.

The *Kao* reference discloses initial values (**Figure 9** note the values inside the blocks *RA*, *RB*, *YA* and *YB*, **Figure 13** note the values in the *YA* block being shifted out, **Col. 3 Lines 49-53**, **Col. 3 Lines 63-67**, **Col. 4 Lines 1-2**), and adding a feedback, recursive value, (**Figure 8**, note the arrows going from the output of the *MUX3/MUL3* block back into the parallel *WRAA* and *WRAB* blocks, this is feedback **Col. 2 Lines 12-13**, **Col. 2 Lines 22-47** note the phrase "Recursive multiplication and division" recursion requires feedback in order to function, **Col. 5 Lines 27-38**).

8. Dependent **Claims 27-30, 32, 34, 35, 37-40, 42, 44 and 45** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Tomizawa et al. U.S. Patent 5,574,717** in view of **Foxcroft U.S. Patent 5,818,855**.

8.1 As regards independent **Claims 26 and 36** see paragraph 6 above.

8.2 As regards dependent **Claims 27 and 37** the *Tomizawa et al.* reference does not expressly disclose the, *well known in the art method*, of using a hardware description language to design a high-speed communications circuit with forward error correction, however the *Tomizawa et al.* reference does disclose implementation in hardware of parallel equations (**Figure 15**).

The *Foxcroft* reference discloses using a hardware description language to high-speed communications circuit with forward error correction (**Col. 2 Lines 18-37, EXAMPLE, Col. 7, 8, 9 & 10**).

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have used a hardware description language to design a high-speed communications circuit because, hardware description languages are flexible design tools that allow for simulation using *test benches*, and provide compatibility with other modern design methodologies to verify modern circuit designs, in such a manner that, to design a high-speed circuit using legacy methodologies would be cost prohibitive and to inefficient to be considered practical.

8.3 As regards dependent **Claims 28 and 38** the *Tomizawa et al.* reference does not expressly disclose using software to design a circuit, however the *Tomizawa et al.* reference does disclose implementation in hardware of parallel equations (**Figure 15**).

The *Foxcroft* reference discloses using software, to design a high speed serial communications circuit (**Col. 2 Lines 18-37, EXAMPLE, Col. 7, 8, 9 & 10**).

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have used a hardware description language to design a high-speed communications circuit because, hardware description languages are flexible design tools that allow for simulation using *test benches*, and provide compatibility with other modern design methodologies to verify modern circuit designs, in such a manner that, to design a high-speed circuit using legacy methodologies would be cost prohibitive and to inefficient to be considered practical.

8.4 As regards dependent **Claims 29 and 39** the *Tomizawa et al.* reference does not expressly disclose *strings*.

The *Foxcroft* reference discloses storing a plurality of “strings” of data in a plurality of storage elements (**Figure 5, Figure 7 Items 70, 60, 62, 64, 66, Col. 4 Lines 32-45**), where the plurality of “strings” represent a plurality of initial values of a circuit (**Col. 3 Lines 18-45**), storing the “strings” in data structures (**Col. 7, 8, 9 & 10**), where the “strings” represent mathematical operations (**Figure 1, Col. 4 Lines 7-67, Col. 5 and Col. 6 Lines 1-39**).

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have used a hardware description language methods, as disclosed in the *Foxcroft* reference, to design a high-speed communications circuit because, hardware description languages are flexible design tools that allow for simulation using *test benches*, and provide compatibility with other modern design methodologies to verify modern circuit designs, in such a manner that, to design a high-speed circuit using legacy methodologies would be cost prohibitive and to inefficient to be considered practical.

8.5 As regards dependent **Claims 30 and 40** the *Tomizawa et al.* reference does not expressly disclose “XOR” or “AND” for addition and multiplication.

The *Foxcroft* reference discloses both “XOR” for addition and “AND” for multiplication (**Figure 11 and Figure 10, Col 6 Lines 35-39, Col. 7 Lines 15-17**).

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have used a hardware description language methods, as disclosed in the *Foxcroft* reference, to design a high-speed communications circuit because, hardware description languages are flexible design tools that allow for simulation using *test benches*, and provide compatibility with other modern design methodologies to verify high density circuit designs, in

such a manner that, to design a high-speed circuit using legacy methodologies, would be cost prohibitive and to inefficient to be considered practical.

8.6 As regards dependent **Claims 32 and 42** the *Tomizawa et al.* reference does not expressly disclose designing an ASIC.

The *Foxcroft* reference discloses designing an ASIC (**Col. 1 Lines 52-55, Col. 9 Lines 34-37**).

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have implemented the design in an ASIC (Application Specific Integrated Circuit) because of the increased performance available from using an ASIC as opposed to a Field Programmable Gate Array (*Tomizawa et al.* reference **Col. 3 Lines 34-45**).

8.7 As regards dependent **Claims 34 and 44** the *Tomizawa et al.* reference does not expressly disclose BCH code used for Forward Error Correction.

The *Foxcroft* reference discloses using a BCH code for Forward Error Correction (**Col. 2 Lines 18-37**).

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have used a BCD code for Forward Error Correction so that the communications system of the *Tomizawa et al.* reference would be compatible with the DRAFT ETS 300 744 (May 1996) standard, (**Foxcroft Col. 1 Lines 19-34**).

8.8 As regards dependent **Claims 35 and 45** the *Tomizawa et al.* reference discloses parallel equations and feedback (**Figure 17 and Col. 11 & 12 “Sixth Embodiment”**).

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9. Dependent **Claims 33 and 43** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Tomizawa et al. U.S. Patent 5,574,717** in view of **Foxcroft U.S. Patent 5,818,855** and in further view of **Oskouy et al. U.S. Patent 5,673,279**.

9.1 As regards independent **Claims 26 and 36** see section 6 above.

9.2 As regards dependent **Claims 27 and 32** please see sections 8.2 and 8.6 above.

9.3 As regards dependent **Claim 42** please see section 8.6 above.

9.4 As regards dependent **Claims 33 and 43** the *Tomizawa et al.* reference does not expressly disclose verifying a circuit design.

The *Oskouy et al.* reference discloses verifying a circuit design (**Figure 7, Col. 1 Lines 13-22, Col. 3 Lines 19-21**).

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made to verify the functioning of an ASIC during the design and simulation phase of product development because of the need to verify that the circuit design is working correctly before incurring the large cost involved in manufacturing an ASIC at a chip fabrication facility.

10. Dependent **Claims 31 and 41** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Tomizawa et al. U.S. Patent 5,574,717** in view of **Foxcroft U.S. Patent 5,818,855** and in further view of **Kao U.S. Patent 5,642,367**.

10.1 As regards independent **Claims 26 and 36** see section 6 above.

10.2 As regards dependent **Claims 28** see section 8.3 above.

10.3 As regards dependent **Claims 37 and 38** see sections 8.2 and 8.3 above.

10.4 As regards dependent **Claims 31 and 41** the *Tomizawa et al.* reference does not expressly disclose a plurality of cycles being simulated.

The *Kao* reference discloses that in order to properly simulate a *forward error correcting* circuit design that the circuit performing the calculations of a *Galois* field must operate for a plurality of cycles (**Col. 8 Lines 58-67 and Col. 9 Lines 1-18**).

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made to have a serial communications circuit perform for a plurality of cycles because, in order to calculate a *Galois* field because multiplication is performed in digital logic using shift registers and in order to shift the values inside these shift registers and *multiply* them then the shift register must be clocked a *plurality of cycles*.

Conclusion

11. **Claims 1-45** have been presented for Examination. **Claims 1-45** have been Examined and rejected. This action is **NON-Final**.

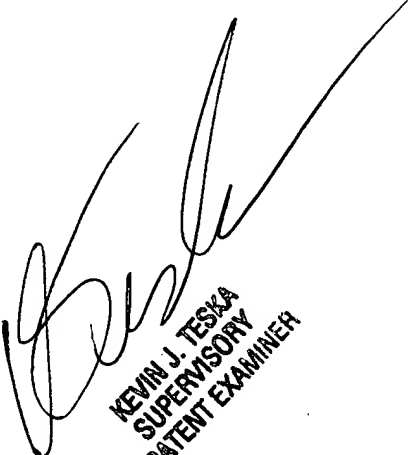
11.1 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwain M Craig whose telephone number is 703 305-7150. The examiner can normally be reached on 10:00 - 6:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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DMC



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